What Is Claimed Is:

1. A reset pulse generator for a CPU, which generating an oscillating disable signal after initialization, comprising:

an oscillating circuit coupled to the CPU to output a sequence of reset pulses to the CPU; and

an oscillating disable circuit coupled to the oscillating circuit for disabling the oscillating circuit and initiating normal mode CPU operation when the oscillating disable signal is received.

2. The reset pulse generator as claimed in claim 1, wherein the oscillating circuit comprises:

a Schmitt trigger having an input terminal and an output terminal;

a resistor coupled between the input terminal and the output terminal; and

a capacitor coupled to the input terminal and a ground level.

3. The reset pulse generator as claimed in claim 1, wherein the oscillating disable circuit is a switch turned on by the oscillating disable signal to stop oscillation of the oscillating circuit.

4. The reset pulse generator as claimed in claim 1, further comprising a manual switch to generate a start signal to enable the oscillating circuit.

5. The reset pulse generator as claimed in claim 1, wherein the start signal is generated during power on.

6. A reset pulse generator, comprising:

a CPU for generating an oscillating disable signal after initialization;

an oscillating circuit coupled to the CPU to output a sequence of reset pulses to the CPU; and

an oscillating disable circuit coupled to the oscillating circuit for disabling the oscillating circuit and initiating normal mode CPU operation when the oscillating disable signal is received.

7. The reset pulse generator as claimed in claim 6, wherein the oscillating circuit comprises:

a Schmitt trigger having an input terminal and an output terminal;

a resistor coupled between the input terminal and the output terminal; and

a capacitor coupled to the input terminal and a ground level.

8. The reset pulse generator as claimed in claim 6, wherein the oscillating disable circuit is a switch turned on by the oscillating disable signal to stop oscillation of the oscillating circuit.

9. The reset pulse generator as claimed in claim 6, further comprising a manual switch to generate a start signal to enable the oscillating circuit.

10. The reset pulse generator as claimed in claim 6, wherein the start signal is generated during power on.